WHAT IS CLAIMED IS:

1. A method of populating a data structure having a number of slots for entries represented by N, N being expressible as a power of two with an exponent x, and having a number of entries already entered into the slots represented by L, comprising:

swapping x bits of a binary representation of L; and

using a value obtained by the swapping as an index for a new entry.

2. The method of claim 1, wherein swapping includes exchanging the x bits of the binary representation of L around an axis located at one of a center at a middle bit of the x bits of the binary representation of L when x is an odd number and a center between two middle bits of the x bits of the binary representation of L when x is an even number.

3. The method of claim 2, wherein the middle bit is a bit of the x bits wherein there is an equal number of the x bits on either side of the middle bit.

4. The method of claim 2, wherein the center between two middle bits is a position wherein an equal number of the x bits lie on either side.

5. The method of claim 1, wherein the x bits range from two to the zero power to two to the x minus one power of the binary representation of L.

6. The method of claim 1, wherein using a value obtained by the swapping as an index includes entering an identifier that serves as a pointer to a first component of a sub-stream in a slot corresponding to the value.

7. The method of claim 1, wherein the data structure includes a table in a scheduler.

8. The method of claim 7, wherein the table is a port shaper table.

9. The method of claim 1, wherein the entries are associated with components of at least one existing sub-stream and the new entry is associated with a first component of a new sub-stream.

10. The method of claim 9, wherein the new sub-stream has a series of consecutive components and the new entry is associated with the first component of the new sub-stream, the method further comprising deriving an index value for each consecutive component of the new sub-stream following the first component by adding a consecutive integer multiple of a step to the value obtained by swapping to identify a slot in the table for each consecutive entry of the new sub-stream.

11. The method of claim 10, wherein the new sub-stream includes constant bandwidth traffic associated with a particular port on a network device.

12. The method of claim 11, wherein the traffic includes real-time data traffic.

13. The method of claim 9, wherein the new sub-stream has the largest number of components for entry into the data structure of a plurality of new sub-streams.

14. The method of claim 9, wherein the first component of the new sub-stream includes an ATM cell.

15. The method of claim 9, wherein the first component of the new sub-stream is associated with a particular port on a network device.

16. A method of deriving a plurality of index values for a plurality of entries to be entered into a data structure, the data structure having a number of slots for entries represented by N, N is expressible as a power of 2 with an exponent x, having a number of entries already entered L, and having a number of new entries to be entered into the data structure associated with a plurality of

components of a sub-stream, comprising:

swapping x bits of a binary representation of L to obtain a value L' to obtain an index value associated with a first component of the sub-stream; and

adding an incremented integer multiplied by a step between consecutive entries to L' to obtain an index value associated with subsequent components of the sub-stream.

17. The method of claim 16, further comprising populating the data structure with a pointer to one of the new entries at each index value.

18. The method of claim 16, wherein the data structure is a table in a scheduler.

19. A scheduler comprising:

a memory device to store a table, the table to have a plurality of slots equal to two to the power x for entries, the number of the plurality of slots represented by N, and to have a number of entries already entered into the slots represented by L; and

a processor coupled to the memory device, the processor to derive an index value L' for a component of a sub-stream, the index indicating a slot of the table into which an entry associated with the component of the sub-stream is to be placed, by swapping x bits of a binary representation of the number of entries L already in the table.

20. The scheduler of claim 19, wherein the entry associated with a sub-stream is a first entry of a series of consecutive entries associated with consecutive components of the sub-stream, and wherein the processor is further to derive an index value for each of the consecutive entries following the first entry by adding a progressively incremented integer multiple, starting with a multiple of one, of a step associated with the sub-stream, to L' for each consecutive component, respectively.

21. The scheduler of claim 19, wherein the processor is to derive the index value L' by exchanging x bits of the binary representation of L around an axis located at one of a center bit of the x bits of the binary representation of L when x is an odd number and between two center bits of the x bits of the binary representation of L when x is an even number.

22. The scheduler of claim 19, wherein the component of the sub-stream is a first component in a series of consecutive components associated with the sub-stream, and wherein the processor derives an index value associated with an entry for each of the components, the index values separated by a step associated with the sub-stream.

23. The scheduler of claim 19, wherein the sub-stream includes constant bandwidth traffic associated with a port coupled to the processor.

24. The scheduler of claim 19, wherein the processor is further to place an identifier in the index that points to a component of the sub-stream stored in a second table.

25. An ATM switch comprising:

a port coupled to a network and receiving a sub-stream therefrom, the sub-stream having a plurality of consecutive components;

a memory device to store a table, the table to have a plurality of slots equal to two to the power x for entries, the number of the plurality of slots represented by N, and to have a number of entries already entered into the slots represented by L; and

a processor coupled to the memory device, the processor to derive an index value L' for a component of a sub-stream, the index indicating a slot of the table into which an entry associated with the component of the sub-stream is to be placed, by swapping x bits of a binary representation of the number of entries L already in the table.

26. The ATM switch of claim 25, wherein the entry associated with a sub-stream is a first entry of a series of consecutive entries associated with consecutive components of the sub-stream, and wherein the processor is further to derive an index value for each of the consecutive entries following the first entry by adding a progressively incremented integer multiple, starting with a multiple of one, of a step associated with the sub-stream, to L' for each consecutive component, respectively.

27. The ATM switch of claim 25, wherein the sub-stream includes constant bandwidth traffic associated with the port.

28. The ATM switch of claim 25, wherein the processor is further to place an identifier in the index that points to a component of the sub-stream stored in a second table.

29. An article of manufacture comprising:

a computer readable medium having stored thereon instructions which, when executed, cause a processor to populate a data structure having a number of slots for entries represented by N, N being expressible as a power of two with an exponent x, and having a number of entries already entered into the slots represented by L by:

swapping x bits of a binary representation of L; and

using a value obtained by the swapping as an index for a new entry.

30. The computer readable medium of claim 29, further comprising an instruction stored thereon which, when executed, causes the processor to enter an identifier that serves as a pointer to a first component of a sub-stream in a slot corresponding to the value.